UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/849,022 | 05/20/2004 | Hiroyasu Kiba | 500.43870X00 | 7040 |

24956 7590 02/10/2006

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

| EXAMINER | |
|---|---|
| GOLDEN, JAMES R | |
| **ART UNIT** | **PAPER NUMBER** |
| 2187 | |

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/849,022 | KIBA ET AL. | |
| | Examiner | Art Unit | |
| | James Golden | 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-6 and 8-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6 and 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/7/04,8/2/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

The instant application 10/849022 has a total of 9 claims pending. There are 3 independent claims and 6 dependent claims. Claims 1, 3-5 and 11 are rejected under statutory basis. Claims 1, 3-6 and 8-11 are rejected in view of prior art.

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

2. The information disclosure statements submitted on 10/07/2004 and 08/02/2005 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

### *Drawings*

3. The drawings are objected to because "reflected" in 408 of Fig. 4 should perhaps be corrected to --unreflected--; see the corresponding objection to the specification.

4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is

being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title "Cache Flush Based on Checkpoint Timer" is suggested.

6. The abstract of the disclosure is objected to because "as result" (line 3) should be corrected to --as a result--. Correction is required. See MPEP § 608.01(b).

7. The disclosure is objected to because of the following informalities: "unreflected" [0016, line 21] should be corrected to --reflected-- as in 408 of Fig. 4. Additionally, throughout the disclosure "check point" and "checkpoint" are

used to describe the same concept; a uniform spelling should be used.

Appropriate correction is required.

### *Claim Objections*

8. **Claims 6 and 8-10** are objected to under 37 CFR 1.75 as being substantial duplicates of claims 1 and 3-5, respectively. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). The examiner recognizes the only difference between the two sets of claims, as exemplified by this difference specifically between claims 1 and 6, is the phrase "said storage unit includes: means responsive to..."; if the applicant wishes to use the means plus function construction for these claims, the wording must be corrected to read --said storage unit includes: means for responding to...--

### *Claim Rejections - 35 USC § 112*

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. **Claims 1 and 3-5** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for reciting a use without any active, positive steps delimiting how this use is actually practiced. A method claim should at least recite a positive, active step(s) so that the claim will "set out and circumscribe a particular

area with a reasonable degree of precision and particularity," In re Moore , 58 CCPA 1042, 439 F.2d 1232, 169 USPQ 236 (1971), and make it clear what subject matter these claims encompass, In re Hammack , 57 CCPA 1225, 1230, 427 F.2d 1378, 1382, 166 USPQ 204 (1970), as well as making clear the subject matter from which others would be precluded, In re Hammack, supra , 57 CCPA at 1231, 427 F.2d at 1382, 166 USPQ at 208 . Without reciting any active, positive steps, claims 1-5 fail to achieve these purposes.

### *Claim Rejections - 35 USC § 101*

11. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

12. **Claim 11** is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The entire claim recites the operational design or configuration of the program and fails to embody the program (an example of functional descriptive material) on an appropriate computer-readable storage medium.

13.

### *Claim Rejections - 35 USC § 103*

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been

obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. **Claims 1, 3-6 and 8-11** are rejected under 35 U.S.C. 103(a) as being anticipated over Prabhakaran (US 5,922,040) in view of Kano et al. (US 6,088,773).

16. **With respect to claim 1**, Prabhakaran discloses a cache control method in a data processing system having

- a computer (616 of Fig. 2; column 5, lines 26-27) for executing a program (DBFUPDATE is a process: column 5, line 32), and
- a storage unit (802 of Fig. 4; column 8, line 16) having
  - a memory for storing data transmitted as a result of execution of said program (815 of Fig. 4; column 9, lines 61-63)
  - a disk device for storing data stored in said memory (807 of Fig. 4; column 9, lines 61-63),
- wherein said storage unit
  - responds to an input of a request for storing data transmitted from said program to store the transmitted data in said memory (column 10, lines 18-20) and
  - responds to an input of a request for flushing transmitted from said program to store, in said disk device, the data stored in said memory (column 26, lines 3-4),

- wherein said flush request is transmitted from said program to said storage unit at the timing of a check point in a transaction process operated by said program (column 26, lines 3-4).

Prabhakaran does not disclose the limitation wherein

- said storage unit has
    - a cache memory for storing data transmitted as a result of execution of said program,
- wherein said storage unit
    - responds to an input of a request for storing data transmitted from said program to store the transmitted data in said cache memory and
    - responds to an input of a request for flushing transmitted from said program to store the data stored in said cache memory.

However, Kano et al. disclose a data processing system with

- a storage unit having a cache memory for storing data transmitted as a result of execution of said program (20 of Fig. 1; column 6, lines 29-32)
- wherein said storage unit
    - responds to an input of a request for storing data transmitted from said program to store the transmitted data in said cache memory (column 6, lines 60-61) and
    - responds to an input of a request for flushing transmitted from said program to store the data stored in said cache memory (column 7, lines 4-7),

Prabhakaran and Kano et al. are analogous art because they are from the same field of endeavor, namely data flushing.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the timed data flushing of Prabhakaran with the cache memory of Kano et al. The motivation for doing so would have been for a "rollback/recovery step for invalidating all the cache blocks in case of a fault, causing the main memory restoring means of the checkpoint acquisition accelerating apparatus to restore the main memory to the state of the most recent checkpoint" (column 4, lines 33-37).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Kano et al. with Prabhakaran for the benefit of timed data flushing from a cache memory to a disk to obtain the invention as specified in claim 1.

17. **With respect to claim 3**, Prabhakaran in view of Kano et al. disclose the cache control method according to claim 1 (see above paragraph 16). Prabhakaran does not disclose the limitations wherein

- each of said data storing request and flush request includes area identification information for specifying areas in said cache memory, and
- wherein when said data storing request is inputted, said transmitted data is stored in an area specified by the area identification information of said data storing request and
- when said flush request is inputted, the data stored in the area specified by the area identification information of said data storing request is stored in said disk device.

However, Kano et al. disclose the limitations wherein

- each of said data storing request (column 13, lines 11-12; if the processor is updating a specific address, the address must be in the request, and the address specifies an area in the memory) and flush request (column 3, lines 38-44; the address specifies an area in the memory) includes area identification information for specifying areas in said cache memory , and
- wherein when said data storing request is inputted, said transmitted data is stored in an area specified by the area identification information of said data storing request (column 13, lines 11-12) and
- when said flush request is inputted, the data stored in the area specified by the area identification information of said data storing request is stored in said disk device (column 3, lines 38-44).

Prabhakaran and Kano et al. are analogous art because they are from the same field of endeavor, namely data flushing.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the timed data flushing of Prabhakaran with the address component of the store and flush commands of Kano et al. The motivation for using an address in the store command would have been such that if an address in a particular cache block is updated more than once, the block can be flagged (column 3, line 59 -- column 4, line 7). The motivation for using an address in the flush command would have been because "where a fault occurs in the computer, the cache memory is invalidated so that the normal data

processing can be resumed from the state of the most recent checkpoint" (column 2, lines 11-14).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Kano et al. with Prabhakaran for the benefit of addresses in store and flush commands to obtain the invention as specified in claim 3.

18. **With respect to claim 4**, Prabhakaran in view of Kano et al. disclose the cache control method according to claim 3 (see above paragraph 17). Prabhakaran does not disclose the limitations wherein

- the area of said cache memory is managed as to whether data update occurs in said area or not, and when said flush request is inputted, data resulting from update of the data stored in the area specified by the area identification information of said data storing request is stored in said disk device.

However, Kano et al. disclose the limitations wherein

- the area of said cache memory is managed as to whether data update occurs in said area or not, and when said flush request is inputted, data resulting from update of the data stored in the area specified by the area identification information of said data storing request is stored in storage (column 3, lines 38-44).

Prabhakaran disclose the limitation wherein the storage is said disk device (column 26, lines 3-4).

Prabhakaran and Kano et al. are analogous art because they are from the same field of endeavor, namely data flushing.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the timed data flushing of Prabhakaran with the flushing of updated cache data of Kano et al. The motivation for flushing updated cache would have been because after a fault "it is necessary to restore the data in the main memory which has been updated after the most recent checkpoint" (column 1, lines 65-67), whereby checkpoints are created when "all the updated data stored in the cache memory are written-back into the main memory" (column 1, lines 61-62).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Kano et al. with Prabhakaran for the benefit of flushing the updated cache addresses to obtain the invention as specified in claim 4.

19. **With respect to claim 5**, Prabhakaran in view of Kano et al. disclose the cache control method according to claim 3 (see above paragraph 17). Prabhakaran does not disclose the limitations wherein the cache control method according to claim 3, wherein the area identification of said cache memory includes volume identification and segment identification information.

However, Kano et al. disclose the limitations wherein the cache control method according to claim 3, wherein the area identification of said cache memory includes volume identification (the "cache blocks") and segment identification information (the "addresses") (column 3, lines 38-44; the addresses contain volume information in that they identify a particular cache block).

Prabhakaran and Kano et al. are analogous art because they are from the same field of endeavor, namely data flushing.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the timed data flushing of Prabhakaran with the cache addressing of Kano et al. The motivation for this type of cache addressing would have been because "where a fault occurs in the computer, the cache memory is invalidated so that the normal data processing can be resumed from the state of the most recent checkpoint" (column 2, lines 11-14).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Kano et al. with Prabhakaran for the benefit of cache addressing to obtain the invention as specified in claim 5.

20. **With respect to claim 6**, Prabhakaran discloses a cache control method in a data processing system having

- a computer (616 of Fig. 2; column 5, lines 26-27) for executing a program (DBFUPDATE is a process: column 5, line 32), and
- a storage unit (802 of Fig. 4; column 8, line 16) having
    - a memory for storing data transmitted as a result of execution of said program (815 of Fig. 4; column 9, lines 61-63)
    - a disk device for storing data stored in said memory (807 of Fig. 4; column 9, lines 61-63),
- wherein said storage unit includes
    - means responsive to an input of a request for storing data transmitted from said program to store the transmitted data in said memory (column 10, lines 18-20) and

- means responsive to an input of a request for flushing transmitted from said program to store, in said disk device, the data stored in said memory (column 26, lines 3-4),

- wherein said flush request is transmitted from said program to said storage unit at the timing of a check point in a transaction process operated by said program (column 26, lines 3-4).

Prabhakaran does not disclose the limitation wherein

- said storage unit has
  - a cache memory for storing data transmitted as a result of execution of said program,
- wherein said storage unit includes
  - means responsive to an input of a request for storing data transmitted from said program to store the transmitted data in said cache memory and
  - means responsive to an input of a request for flushing transmitted from said program to store the data stored in said cache memory.

However, Kano et al. disclose a data processing system with

- a storage unit having
  - a cache memory for storing data transmitted as a result of execution of said program (20 of Fig. 1; column 6, lines 29-32)
- wherein said storage unit includes

- means responsive to an input of a request for storing data transmitted from said program to store the transmitted data in said cache memory (column 6, lines 60-61) and
- means responsive to an input of a request for flushing transmitted from said program to store the data stored in said cache memory (column 7, lines 4-7),

Prabhakaran and Kano et al. are analogous art because they are from the same field of endeavor, namely data flushing.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the timed data flushing of Prabhakaran with the cache memory of Kano et al. The motivation for doing so would have been for a "rollback/recovery step for invalidating all the cache blocks in case of a fault, causing the main memory restoring means of the checkpoint acquisition accelerating apparatus to restore the main memory to the state of the most recent checkpoint" (column 4, lines 33-37).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Kano et al. with Prabhakaran for the benefit of timed data flushing from a cache memory to a disk to obtain the invention as specified in claim 1.

21. **With respect to claim 8**, Prabhakaran in view of Kano et al. disclose the cache control method according to claim 6 (see above paragraph 20). Prabhakaran does not disclose the limitations wherein

- each of said data storing request and flush request includes area identification information for specifying areas in said cache memory, and

- wherein when said data storing request is inputted, said transmitted data is stored in an area specified by the area identification information of said data storing request and
- when said flush request is inputted, the data stored in the area specified by the area identification information of said data storing request is stored in said disk device.

However, Kano et al. disclose the limitations wherein

- each of said data storing request (column 13, lines 11-12; if the processor is updating a specific address, the address must be in the request, and the address specifies an area in the memory) and flush request (column 3, lines 38-44; the address specifies an area in the memory) includes area identification information for specifying areas in said cache memory , and
- wherein when said data storing request is inputted, said transmitted data is stored in an area specified by the area identification information of said data storing request (column 13, lines 11-12) and
- when said flush request is inputted, the data stored in the area specified by the area identification information of said data storing request is stored in said disk device (column 3, lines 38-44).

Prabhakaran and Kano et al. are analogous art because they are from the same field of endeavor, namely data flushing.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the timed data flushing of Prabhakaran with the address component of the store and flush commands of Kano et al. The

motivation for using an address in the store command would have been such that if an address in a particular cache block is updated more than once, the block can be flagged (column 3, line 59 -- column 4, line 7). The motivation for using an address in the flush command would have been because "where a fault occurs in the computer, the cache memory is invalidated so that the normal data processing can be resumed from the state of the most recent checkpoint" (column 2, lines 11-14).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Kano et al. with Prabhakaran for the benefit of addresses in store and flush commands to obtain the invention as specified in claim 3.

22. **With respect to claim 9**, Prabhakaran in view of Kano et al. disclose the cache control method according to claim 8 (see above paragraph 21). Prabhakaran does not disclose the limitations wherein

- the area of said cache memory is managed as to whether data update occurs in said area or not, and when said flush request is inputted, data resulting from update of the data stored in the area specified by the area identification information of said data storing request is stored in said disk device.

However, Kano et al. disclose the limitations wherein

- the area of said cache memory is managed as to whether data update occurs in said area or not, and when said flush request is inputted, data resulting from update of the data stored in the area specified by the area

identification information of said data storing request is stored in storage (column 3, lines 38-44).

Prabhakaran disclose the limitation wherein the storage is said disk device (column 26, lines 3-4).

Prabhakaran and Kano et al. are analogous art because they are from the same field of endeavor, namely data flushing.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the timed data flushing of Prabhakaran with the flushing of updated cache data of Kano et al. The motivation for flushing updated cache would have been because after a fault "it is necessary to restore the data in the main memory which has been updated after the most recent checkpoint" (column 1, lines 65-67), whereby checkpoints are created when "all the updated data stored in the cache memory are written-back into the main memory" (column 1, lines 61-62).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Kano et al. with Prabhakaran for the benefit of flushing the updated cache addresses to obtain the invention as specified in claim 4.

23. **With respect to claim 10**, Prabhakaran in view of Kano et al. disclose the cache control method according to claim 8 (see above paragraph 21). Prabhakaran does not disclose the limitations wherein the area identification of said cache memory includes volume identification and segment identification information.

However, Kano et al. disclose the limitations wherein the cache control method according to claim 3, wherein the area identification of said cache memory includes volume identification (the "cache blocks") and segment identification information (the "addresses") (column 3, lines 38-44; the addresses contain volume information in that they identify a particular cache block).

Prabhakaran and Kano et al. are analogous art because they are from the same field of endeavor, namely data flushing.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the timed data flushing of Prabhakaran with the cache addressing of Kano et al. The motivation for this type of cache addressing would have been because "where a fault occurs in the computer, the cache memory is invalidated so that the normal data processing can be resumed from the state of the most recent checkpoint" (column 2, lines 11-14).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Kano et al. with Prabhakaran for the benefit of cache addressing to obtain the invention as specified in claim 5.

24. **With respect to claim 11**, Prabhakaran discloses a data processing program for functioning a data processing system having

- a computer (616 of Fig. 2; column 5, lines 26-27) for executing a program (DBFUPDATE is a process: column 5, line 32), and
- a storage unit (802 of Fig. 4; column 8, line 16) having
    - a memory for storing data transmitted as a result of execution of said program (815 of Fig. 4; column 9, lines 61-63)

- a disk device for storing data stored in said memory (807 of Fig. 4; column 9, lines 61-63),

- said program causing said storage unit to execute
  - a step of responding to an input of a request for storing data transmitted from said program to store the transmitted data in said memory (column 10, lines 18-20) and
  - a step of responding to an input of a request for flushing transmitted from said program to store, in said disk device, the data stored in said memory (column 26, lines 3-4),
- wherein said flush request is transmitted from said program to said storage unit at the timing of a check point in a transaction process operated by said program (column 26, lines 3-4).

Prabhakaran does not disclose the limitation wherein

- said storage unit has
  - a cache memory for storing data transmitted as a result of execution of said program,
- wherein said storage unit
  - responds to an input of a request for storing data transmitted from said program to store the transmitted data in said cache memory and
  - responds to an input of a request for flushing transmitted from said program to store the data stored in said cache memory.

However, Kano et al. disclose a data processing system with

- a storage unit having a cache memory for storing data transmitted as a result of execution of said program (20 of Fig. 1; column 6, lines 29-32)
- wherein said storage unit
    - responds to an input of a request for storing data transmitted from said program to store the transmitted data in said cache memory (column 7, lines 4-7) and
    - responds to an input of a request for flushing transmitted from said program to store the data stored in said cache memory (column 26, lines 3-4),

Prabhakaran and Kano et al. are analogous art because they are from the same field of endeavor, namely data flushing.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the timed data flushing of Prabhakaran with the cache memory of Kano et al. The motivation for doing so would have been for a "rollback/recovery step for invalidating all the cache blocks in case of a fault, causing the main memory restoring means of the checkpoint acquisition accelerating apparatus to restore the main memory to the state of the most recent checkpoint" (column 4, lines 33-37).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Kano et al. with Prabhakaran for the benefit of timed data flushing from a cache memory to a disk to obtain the invention as specified in claim 1.

***Conclusion***

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Pong et al. (US 6,874,065) teaches a cache flushing mechanism based on a timer;
- Rochberger (US 6,192,043) also teaches a cache flushing mechanism based on a timer;
- Okamoto et al. (US 5,812,757) teaches checkpoints using a cache flush;
- Kurosawa (US 6,418,515) teaches a cache flushing mechanism tied to checkpoint time.
- Ledain et al. (US 6,021,408) teaches a log book that flushes a memory to a disk on at a checkpoint.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James R. Golden
Patent Examiner
Art Unit 2187

January 24, 2006

Brian R. Peyton
Primary Examiner
AU 2187
2/3/06